

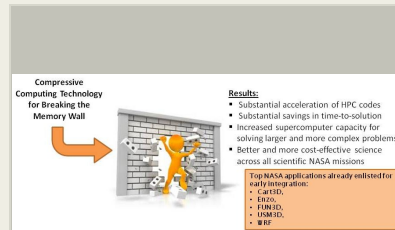
Accelerating Memory-Access-Limited HPC Applications via Novel Fast Data Compression, Phase II

Completed Technology Project (2016 - 2019)



Project Introduction

A fast-paced continual increase on the ratio of CPU to memory speed feeds an exponentially growing limitation for extracting performance from HPC systems. Breaking this memory wall is one of the most important challenges that the HPC community faces today. In Phase I we introduced aggressive innovations enable the injection of unprecedented acceleration into vast classes of memory-access-bound HPC codes via ultra-fast software-based data compression. Groundbreaking speedup on a fully functional NPBCG prototype was delivered to NASA, thus validating the tremendous potential of our approach. The proposed approach is based on a revolutionary theory of compression spearheaded by Accelelogic (Compressive Computing), which is able to provide enormous compressive gains for the typical floating point data of HPC applications. In Phase II we will build on our success with the NPBCG benchmark, and move boldly into tackling the acceleration of a real-life high-profile code, namely NASA's Cart3D, improving its performance by a paradigm-shifting 2x to 4x end-to-end wall-clock time acceleration by the end of Phase II. Our firm has accumulated crucial know-how and has synthesized its expertise into a powerful industrial-quality process for software acceleration that will be used to ensure success on completing Phase II objectives. In Phase II we also plan on injecting a second NASA code with basic Compressive Computing techniques, and providing it with base levels of acceleration of ~1.3-2x. We will choose this second code from a pool of high-profile codes that have already signed up as early adopters for this project: FUN3D, USM3D, Enzo, and WRF. The work on a second NASA code will also serve as the ultimate field test of the broadness and ease-of-infusion of the proposed technology. We have secured complementary funds in the amount of \$500,000 to increase resources and ensure that the proposed Phase II proposed will be successfully accomplished.



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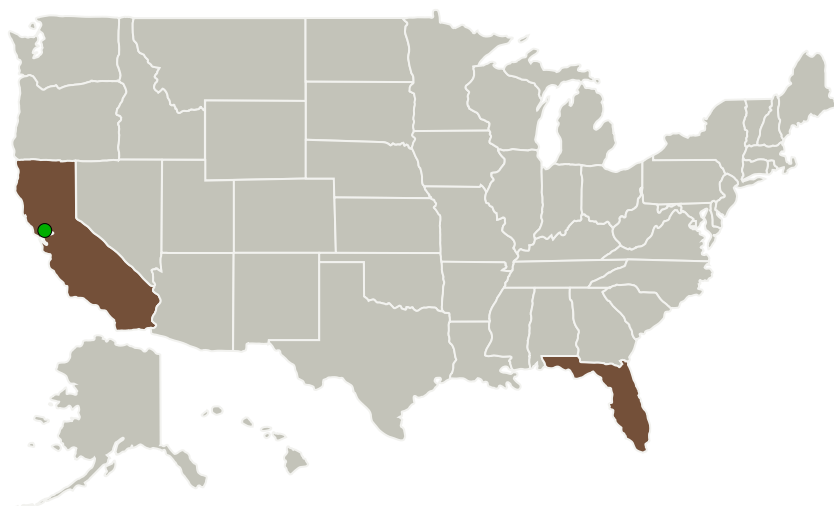
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Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
Accelogic, LLC	Lead Organization	Industry	Weston, Florida
● Ames Research Center(ARC)	Supporting Organization	NASA Center	Moffett Field, California

Primary U.S. Work Locations	
California	Florida

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

Accelogic, LLC

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

Carlos Torrez

Principal Investigator:

Juan G Gonzalez

Co-Investigator:

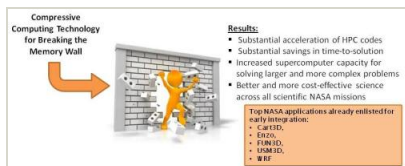
Juan Gonzalez

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Images

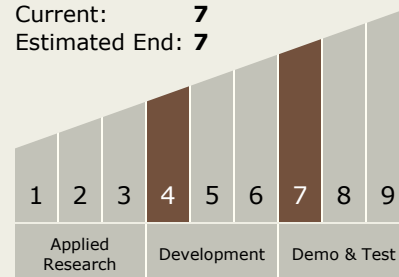


Briefing Chart Image

Accelerating Memory-Access-Limited HPC Applications via Novel Fast Data Compression, Phase II
(<https://techport.nasa.gov/image/132217>)

Technology Maturity (TRL)

Start: 4
Current: 7
Estimated End: 7



Technology Areas

Primary:

- TX11 Software, Modeling, Simulation, and Information Processing
 - TX11.6 Ground Computing
 - TX11.6.2 Automated Exascale Software Development Toolset

Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System